Claims

1. Circuit element, comprising:

- N pairs of transistor units, each pair including a first (MP) and a second (MN) complementary transistor unit with at least four nodes, where the first transistor unit includes
  - a first node, which is connected to an upper (V_{DD}) voltage level,
  - a second node connected to the second node of a complementary transistor unit,
  - an input node that controls the current through, and the voltage over the first and second node,
  - a control input node that controls the current/voltage characteristics of the transistor unit,

  and the second transistor unit includes
  - a first node, which is connected to a lower (V_{SS}) voltage level,
  - a second node connected to the second node of a complementary transistor unit,
  - an input node that controls the current through, and the voltage over the first and second node,
  - a control input node that controls the current/voltage characteristics of the transistor unit,

  where the second nodes of the respective paired transistor units also are connected to each other, and the upper and lower voltage levels (V_{DD}, V_{SS}) are such that the transistor units operate in subthreshold,
- N input terminals (X_1, X_2, .. X_N) connected to input nodes of the respective paired transistor units,
- an output terminal (CN) connected to the interconnected second nodes of the paired transistor units, and
- at least one of the following:
  - a control terminal (BP) connected to the control input nodes of the first transistor units, of the N paired transistors,
  - a control terminal (BN) connected to the control input nodes of the second transistor units, of the N paired transistors,

where N is an integer.

2. Circuit element according to claim 1, **characterized in** that the first transistor units are PMOS transistors, and the second transistors are NMOS transistors.

3. Circuit element according to claim 1 or 2, **characterized in** that the circuit element can be reconfigured in real time, between a logic NAND-function, a logic NOR-function, and a CARRY'-function, by a change in the voltage level of at least one of the control terminals (BN, BP).

4. Circuit element according to claim 1, 2, or 3 **characterized in** that $2 \leq N \leq 8$, preferably $2 \leq N \leq 4$.

5. Threshold element circuit with full adder function, **characterized in** that the circuit comprises two circuit elements according to claim 1, in which circuit elements N is 3, where the output terminal (CN) of the first circuit element is connected to the control terminal (BP) for the PMOS well terminals of the second circuit element, and where the first output, in the form of the carry terminal (C), is connected to the second nodes of a pair of transistor units according to claim 1, where the input terminal of this transistor unit pair is connected to the output terminal (CN) of the first circuit element, and where the second output, in the form of the sum terminal (S), is connected to the second nodes of a pair of transistor units according to claim 1, where the input terminal of this transistor unit pair is connected to the output terminal (SN) of the second circuit element.